LISTING OF CLAIMS

1. (Currently Amended) A circuit for monitoring the state of at least one switch, comprising:

a first monitoring circuit, coupled to a switch, the switch being one of a normally-open switch or a normally-closed switch, comprising:

a normally-open detection circuit coupled to a first terminal of the switch for detecting when the switch, if configured as a normally-open switch, closes and generating a first signal based on the detection; and

a normally-closed detection circuit also coupled to the first terminal of the switch for detecting when the switch, if configured as a normally-closed switch, opens and generating a second signal based on the detection; and

a configuring circuit, coupled to the first monitoring circuit, for configuring the first monitoring circuit to utilize ~~one of~~ the normally-open detection circuit and disable the normally-closed detection circuit if the switch is a normally-open switch or alternatively utilize the normally-closed detection circuit and disable the normally-open detection circuit if the switch is a normally-closed switch ~~based on the switch configuration~~.

2. (Currently Amended) The circuit of claim 1, wherein the normally-closed detection circuit includes a closed-to-open circuit for detecting whether the switch changes from a closed state to an open state and for pulling the ~~[[a]]~~ first terminal of the switch to a voltage representative of one of a logic high state and a logic low state.

3. (Previously Presented) The circuit of claim 2, wherein the closed-to-open circuit is configurable for pulling the first terminal of the switch to a voltage representative of a logic high state and to a logic low state.

4. (Previously Presented) The circuit of claim 3, wherein the closed-to-open circuit comprises:

at least one resistive element;

a first transistor coupled between a first terminal of the at least one resistive element and a high reference voltage source;

a second transistor coupled between the first terminal of the at least one resistive element and the first terminal of the switch;

a third transistor coupled between a second terminal of the at least one resistive element and a low reference voltage source; and

a fourth transistor coupled between the second terminal of the at least one resistive element and the first terminal of the switch.

5. (Previously Presented) The circuit of claim 4, wherein the configuring circuit comprises control circuitry for activating the first transistor and the third transistor at substantially the same time, or activating the second transistor and the fourth transistor at substantially the same time.

6. (Original) The circuit of claim 5, wherein the control circuitry comprises a register.

7. (Previously Presented) The circuit of claim 5, wherein the configuring circuit comprises control circuitry for selectively activating one of the first transistor and the third transistor while occasionally activating the other of the first and third transistors, or for selectively activating one of the second transistor and the fourth transistor while occasionally activating the other of the second and fourth transistors.

8. (Currently Amended) The circuit of claim 1, wherein the normally-open detection circuit includes a open-to-closed circuit for detecting whether the switch changes from an open state to a closed state and for relatively weakly pulling the ~~[[a]]~~ first terminal of the switch towards a voltage representative of one of a logic high state and a logic low state.

9. (Previously Presented) The circuit of claim 8, wherein the open-to-closed circuit is configurable for pulling the first terminal of the switch to a voltage representative of a logic high state and to a logic low state.

10. (Previously Presented) The circuit of claim 9, wherein the open-to-closed circuit comprises at least one first transistor coupled between a high reference voltage level and the first terminal of the switch, at least one second transistor coupled between a low reference voltage level and the first terminal of the switch, and control logic for generating at least one control signal having a value indicative of a configuration of the open-to-closed circuit, a control terminal of each of the at least one first transistor and the at least one second transistor having a value based upon the value of the at least one control signal.

11. (Previously Presented) The circuit of claim 10, wherein the open-to-closed circuit comprises a first detection circuit having an input coupled to the first terminal of the switch and an output coupled to a control terminal of the at least one first transistor, the at least one control signal being coupled to an input of the first detection circuit, the output of the first detection circuit having a value indicative of the first detection circuit detecting the first terminal of the switch being pulled to a voltage representative of a logic low level.

12. (Original) The circuit of claim 11, wherein the first detection circuit comprises a logic gate with hysteresis.

13. (Previously Presented) The circuit of claim 11, wherein the open-to-closed circuit further comprises a second detection circuit having an input coupled to the first terminal of the switch and an output coupled to a control terminal of the at least one second transistor, the at least one control signal being coupled to an input of the second detection circuit, the output of the second detection circuit having a value indicative of the second detection circuit detecting the first terminal of the switch being pulled to a voltage representative of a logic high value.

14. (Previously Presented) The circuit of claim 13, wherein the open-to-closed circuit further comprises an output circuit having a first input coupled to the output of the first detection circuit, a second input coupled to the output of the second detection circuit, and an output having a value representative of one of the first and second detection circuits detecting the switch being closed.

15. (Currently Amended) The circuit of claim 1, wherein the circuit further comprises:

a second monitoring circuit, coupled to a second switch, the second switch being one of a normally-open switch or a normally-closed switch, comprising:

a second normally-open detection circuit coupled to a first terminal of the second switch for detecting when the second switch, if configured as a normally-open switch, closes and generating a third signal based on the detection; and

a second normally-closed detection circuit also coupled to the first terminal of the switch for detecting when the second switch, if configured as a normally-closed switch, opens and generating a fourth signal based on the detection, wherein the configuring circuit is coupled to the second monitoring circuit, for configuring the second monitoring circuit to utilize ~~one of~~ the second normally-open detection circuit and disable the second normally-closed detection circuit if the second switch is a normally-open switch or alternatively utilize the second normally-closed detection circuit and disable the second normally-open detection circuit if the second switch is a normally-closed switch ~~based on the second switch configuration~~.

16. (Previously Presented) A method for detecting the state of at least one switch using a circuit, comprising:

configuring a circuit, coupled to a switch, based on whether the switch is a normally-open switch or a normally-closed switch, wherein configuring the circuit comprises:

activating a normally-open detection circuit and deactivating a normally-closed detection circuit if the switch is a normally-open switch; and

activating the normally-closed detection circuit and deactivating the normally-open detection circuit if the switch is a normally-closed switch;

detecting, by the activated one of the normally-open detection circuit and the normally-closed detection circuit, the switch changing states; and

generating a signal indicative of the detection.

17. (Previously Presented) The method of claim 16, wherein the step of configuring comprises configuring the circuit to relatively weakly pull a terminal of the switch towards a voltage representative of one of a logic high state and a logic low state.

18. (Original) The method of claim 17, wherein the step of configuring comprises activating transistors to couple a resistive element between the terminal of the switch and the selected one of the logic high state and the logic low state.

19. (Original) The method of claim 17, wherein the step of configuring comprises occasionally activating at least one transistor to occasionally couple a resistive element between the terminal of the switch and the selected one of the logic high state and the logic low state.

20. (Previously Presented) The method of claim 16 and further comprising:

configuring a second circuit, coupled to a second switch, based on whether the switch is a normally-open switch or a normally-closed switch,

wherein configuring the circuit comprises:

activating a second normally-open detection circuit and deactivating a second normally-closed detection circuit if the second switch is a normally-open switch; and

activating the second normally-closed detection circuit and deactivating the second normally-open detection circuit if the second switch is a normally-closed switch;

detecting, by the activated one of the second normally-open detection circuit and the second normally-closed detection circuit, the second switch changing states; and

generating a second signal indicative of the detection.

21. (Currently Amended) A system, comprising:

a switch having a first conduction terminal and a second conduction terminal, the switch being one of a normally-open switch or a normally-closed switch;

a first circuit coupled to the first conduction terminal of the switch for detecting the switch opening and generating if activated a signal indicative of that detection;

a second circuit coupled to the first conduction terminal of the switch for detecting the switch closing and generating if activated a signal indicative of that detection;

a third circuit coupled to the first circuit and the second circuit for configuring the first and second circuits by activating ~~one of~~ the first circuit and deactivating the second circuit if the switch is a normally-closed switch and deactivating the ~~other of the~~ first circuit and activating the second circuit if ~~based on whether~~ the switch is a ~~normally-closed switch or a~~ normally-open switch ~~, respectively~~.

22. (Currently Amended) The system of claim 21, wherein the activated first/second circuit is configurable to one of: selectively pull the first conduction terminal of the switch towards a voltage level representative of a logic high state, or ~~and to~~ selectively pull the first conduction terminal of the switch towards a voltage level representative of a logic low state.

23. (Currently Amended) The system of claim 22, wherein the activated circuit selectively weakly pulls the first terminal of the switch towards a certain ~~preselected~~ logic state, relative to a drive strength of the switch to pull the first terminal thereof towards a different logic state.

24. (Original) The system of claim 23, wherein the first circuit comprises:

at least one resistive element;

a first transistor coupled between a first terminal of the at least one resistive element and a high reference voltage source;

a second transistor coupled between the first terminal of the at least one resistive element and the first conduction terminal of the switch;

a third transistor coupled between a second terminal of the at least one resistive element and a low reference voltage source; and

a fourth transistor coupled between the first conduction terminal of the switch and the second terminal of the at least one resistive element.

25. (Original) The system of claim 24, wherein the first circuit further comprises control circuitry for selectively activating the first and third transistors at substantially the same time, and selectively activating the second and fourth transistors at substantially the same time.

26. (Original) The system of claim 24, wherein the first circuit further comprises control circuitry for selectively activating one of the first and third transistors while occasionally activating the other of the first and third transistors, and for selectively activating one of the second and fourth transistors while occasionally activating the other of the second and fourth transistors.